Computer Organization & Architecture

15B11CI313

**Tutorial-6: Addressing Mode**

1. **Consider a three word machine instruction-**

**ADD A[R0], @B**

**The first operand (destination) “A[R0]” uses indexed addressing mode with R0 as the index register. The second operand operand (source) “@B” uses indirect addressing mode. A and B are memory addresses residing at the second and the third words, respectively. The first word of the instruction specifies the opcode, the index register designation and the source and destination addressing modes. During execution of ADD instruction, the two operands are added and stored in the destination (first operand).The number of memory cycles needed during the execution cycle of the instruction is-**

1. **A machine has a 32-bit architecture, with 1-word long instructions. It has 64 registers, each of which is 32 bits long. It needs to support 45 instructions, which have an immediate operand in addition to two register operands. Assuming that the immediate operand is an unsigned integer, the maximum value of the immediate operand is \_\_\_\_\_\_\_\_\_\_\_\_.**
2. **A processor has 40 distinct instructions and 24 general purpose registers. A 32-bit instruction word has an opcode, two register operands and an immediate operand. The number of bits available for the immediate operand field is \_\_\_\_\_\_\_\_\_\_\_\_**
3. **Consider a processor with 64 registers and an instruction set of size twelve. Each instruction has five distinct fields, namely, opcode, two source register identifiers, one destination register identifier, and a twelve-bit immediate value. Each instruction must be stored in memory in a byte-aligned fashion. If a program has 100 instructions, the amount of memory (in bytes) consumed by the program text is \_\_\_\_\_\_\_\_\_\_\_\_**
4. **Consider a hypothetical processor with an instruction of type LW R1, 20(R2), which during execution reads a 32-bit word from memory and stores it in a 32-bit register R1. The effective address of the memory location is obtained by the addition of a constant 20 and the contents of register R2. Which of the following best reflects the addressing mode implemented by this instruction for operand in memory?**
5. **Write a GPR assembly –language program that perform the following computation using five registers R0,R1,R2,R3,R4 only. Final result is in R0.**

**14\*[{9+(3\*8)}-7]**

1. **Write a GPR assembly –language program that perform the following computation using four registers R0,R1,R2,R3 only. Final result is in R0.**

**14\*[{9+(3\*8)}-7]**

**8. Briefly explain the difference between two-operand and three-operand instruction**

**formats.**